REMARKS/ARGUMENTS

The above-identified patent application has been reviewed in light of the Examiner's Action dated March 15, 2005. Claims 1 and 4-6 have been amended and Claim 3 has been cancelled, without intending to abandon or dedicate to the public any patentable subject matter. Accordingly, Claims 1, 2 and 4-11 are now pending.

Claim 1 was rejected as being unpatentable over Thurber, Jr. (U.S. Patent No. 6,169,444). Applicant respectfully traverses this rejection. More specifically, Thurber does not disclose 1) the delay circuit that provides the delayed first clock signal to the second terminal of the capacitor and 2) the timing adjustment circuit that generates the second clock signal based on the delayed first clock signal provided to the second terminal of the capacitor, as recited in Claim 1. Rather, Thurber discloses generating a second clock signal provided to the switches S3 and S4 by delaying a first clock signal provided to the switches S1 and S2 (see Fig. 4). The switches S2 and S4 do not function as the delay circuit of the present invention. In other words, Thurber does not disclose providing a delayed first clock signal to the terminal of the capacitor C-X connected to the node between the switches S2 and S4 and generating a second clock signal provided to the switch S3 based on the delayed first clock signal.

In contrast, the charge pump circuit of the present invention includes the delay circuit (B1 Fig. 3) to increase the voltage conversion efficiency. As shown in Fig. 4 of the present specification, after the gate voltage (ϕT1) of the first transistor (TR1) is determined to a low level to turn off the

first transistor (TR1) and the first transistor surely changes its state from an ON state to an OFF state, the delay circuit (B1) delays the determined voltage (ϕT1) and generates a delayed signal (ϕC1), thereby decreasing a voltage of the node (N1) between the first and second transistors (TR1, TR2) to the low level. Then, the timing adjustment circuit generates the gate voltage (ϕT2) of the second transistor (TR2) based on the delayed signal (ϕC1) provided to the terminal of the capacitor (Cl) connected to the delay circuit. That is, the voltage at the node (N1) and the gate voltage (ϕT2) of the second transistor (TR2) both change after the gate voltage (ϕT1) of the first transistor (TR1) is determined to the low level that turns off the transistor (TR1), which prevents a large through current from flowing through the first and second transistors (TR1, TR2) and guaranties the operation of the charge pump circuit. Accordingly, Applicant believes that the present invention is not obvious in light of Thurber.

Claims 2, 3, 6 and 9 were rejected as being unpatentable over Thurber in view of Mukainakano et al. (U.S. Patent No.6, 107, 862). Applicant respectfully traverses this rejection. Since neither Thurber nor Mukainakano discloses the delay circuit and the timing adjustment circuit of the present invention, Applicant believes that the present invention of Claims 2, 6 and 9 is not obvious in light of Thurber in view of Mukainakano.

Based upon the foregoing, Applicant believes that all pending claims are in condition for allowance and such disposition is respectfully requested. In the event that a telephone conversation would further prosecution and/or expedite allowance, the Examiner is invited to contact the undersigned.

Respectfully submitted,

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